1. A stacked gate flash memory cell, comprising:

a) a floating gate on top of a gate oxide on a semiconductor substrate,

b) a control gate on top of said floating gate separated by an insulating material and forming a stacked gate,

c) a lightly doped drain ion implanted into said substrate on drain side of said stacked gate,

d) a heavily doped source ion implanted into said substrate on source side of said stacked gate,

e) sidewall spacers formed on sides of said stacked gate,

f) a heavily doped drain ion implanted into said substrate adjacent to sidewall spacer on drain side of said stacked gate.

2. The stacked gate flash memory cell of claim 1, wherein said source is heavily doped to affect hot electron programming and Fowler-Nordheim tunneling to erase said floating gate.

3. The stacked gate flash memory cell of claim 2, wherein a double diffused source is used to produce Fowler-Nordheim tunneling.

4. The stacked gate flash memory cell of claim 1, wherein electric field of said drain is greatly reduced as a result of the lightly doped drain reducing hot electron generation at said drain and reducing bit line disturbs.

5. The stacked gate flash memory cell of claim 4, wherein a double diffused drain or a large angle tilted implanted drain can be used in place of said lightly doped drain to reduce hot electron generation at said drain and reducing bit line disturbs.

6. The stacked gate flash memory cell of claim 4, wherein a high drain voltage can be used to increase read current.

7. A method of producing a stacked gate flash memory cell to reduce disturb conditions, comprising:

a) growing a gate oxide on top of a semiconductor substrate,

b) forming a floating gate of a on top of said gate oxide,

c) forming an oxide layer on top of said floating gate,

d) forming a control gate on top of said floating gate with said oxide layer in between to produce a stacked gate,

e) ion implanting a lightly doped drain in said substrate on drain side of said stacked gate using said stacked gate as a mask,

f) ion implanting a heavily doped source in said substrate on source side of said stacked gate using said stacked gate as a mask,

g) forming sidewall spacers on sides of said stacked gate of an insulating material,

h) ion implanting a heavily doped drain in said substrate on drain side of said stacked gate using said sidewall spacer as a mask.

8. The method of claim 7, wherein ion implanting said source is done with a double diffused source.

9. The method of claim 7, wherein ion implanting of said drain is done with a double diffused drain.

10. The method of claim 7, wherein ion implanting said drain is done with a large angle tilted implanted drain.